Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-12 (cancelled)

Claim 13. (currently amended) A non volatile memory, comprising:

a) flash memory cells organized in rows and columns,

b) cells in a row are interconnected by a word line connecting to control gates of said flash memory cells in said row,

c) cell layout in a first column of cells having a same said cell layout in adjacent second and a third column of cells, whereby a first bit line connects to a ~~select and control~~ portion of a channel under a select and control gate of a memory device of said cells in the first column and ~~the~~ a second bit line connects to ~~a stacked gate~~the portion of said channel under a stacked gate of the third column of cells,

d) said bit line extends full length of said columns, laying between said cells of said first and third columns,~~,~~

e) a source line extends full length of said columns, laying between said cells of said first and second columns, whereby said source line connects to ~~a stacked gate~~ the portion of said channel under the stacked gate of the ~~first~~ second column of cells and

the source line connects to ~~a select and control~~ the portion of said channel under the select and control gate of the ~~second~~ first column of cells,

f) ~~a program operation of~~ said flash memory cells organized by a vertical page comprising said memory cells in the first column to perform a program operation, whereby a source line voltage and a bit line voltage of said vertical page are set for said program operation and a word line program voltage is stepped from cell to cell in said first column,

g) ~~an erase operation of~~ said flash memory cells organized by a horizontal block comprising a first row of cells adjacent to a second row of cells to perform an erase operation and whereby all bit lines, source lines and word lines of said horizontal block are coupled to a same low voltage and then word lines coupled to cells in said horizontal block are biased to an erase voltage,

h) said cell layout in said columns allowing vertical page programming and horizontal page/block erase.

14. (previously presented) The non volatile memory of claim 13 wherein, said bit line provide a path to read data stored in said cells when performing a read operation.

15. (previously presented) The non volatile memory of claim 13 wherein, said source line connect to sources of said cells of the first column , connect to drains of said cells of the second column , and connect to source voltages.

Claims 16-25 (canceled)